

REMARKS

The Office Action dated August 10, 2004, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 1, 6 and 8 have been amended. Applicant submits that the amendments made herein are fully supported in the specification and drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 1-9 are pending in the present application and are respectfully submitted for consideration.

Claims 1-9 were rejected under 35 U.S.C. § 102(e) as being anticipated by Braceras (U.S. Patent No. 6,711,076, "Braceras"). Applicants hereby traverse the rejection, as follows.

Claim 1 includes, among others, features including a plurality of memory blocks, each having a plurality of static memory cells, a first local bit line connected to the static memory cells and a first amplifier having its input connected to the first local bit line to amplify voltage of the first local bit line, and a first global bit line connected commonly to outputs of each of the first amplifiers of the memory blocks. In addition, claim 1 includes a feature wherein precharging circuits are connected to both ends of the first global bit line. Applicant respectfully submits that Braceras fails to disclose or suggest such features.

Rather, contrary to the claimed invention, Braceras shows in Figs. 3 and 4 that amplifiers M16-M20 do not have inputs connected to local bit lines BLT and BLC.

Further, as shown in Figs, 3 and 4 of Braceras, precharging circuits are not positioned at both ends of the data line DLT or DLC (i.e., global bit lines). In addition, data lines DLT and DLC in Braceras are not commonly wired to the plurality of memory blocks (Array Column Circuitry), as in the present invention. Instead, the data lines DLT and DLC in Braceras are local lines wired in each Array Column Circuitry. Thus, Braceras fails to disclose or suggest each and every feature of the present invention as recited in claim 1. Accordingly, Applicants respectfully submit that claim 1 is patentable over Braceras and in condition for allowance.

Claim 7 recites, among others, a feature wherein the first global bit line is laid along the direction in which the memory blocks are arranged. In contrast, in Braceras, the wiring direction of the memory block (Array Column Circuitry) is horizontal in the drawing and the wiring direction of the first global bit line DLT and DLC is vertical in the drawing, and thus, the first global bit line and the direction of the memory blocks are orthogonal to each other. Moreover, claim 7 depends from claim 1 and as such, claim 7 should be deemed allowable for the same reasons as claim 1, as well as for the additional subject matter recited therein.

Claims 2-6, 8 and 9 depend from claim 1 and as such, claims 2-6, 8 and 9 should be deemed allowable for the same reasons as claim 1, as well as for the additional subject matter recited therein.


In view of the above, Applicants respectfully submit that each of claims 1-9 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the

claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 1-9 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned representative at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Attorney Docket No. 108397-00107.

Respectfully submitted,


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